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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 14

Application Number: 10/054,605
Filing Date: November 13, 2001
Appellant(s): HU ET AL.

Burton A. Amernick
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 3, 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1 – 5, 7 – 10, 18 – 22, 24 – 27, and 35 – 38 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,695,810	**Dubin et al.**	**12-1997**
6,077,774	**Hong et al.**	**6-2000**
6,372,633	**Maydan et al.**	**4-2002**
6,180,523	**Lee et al.**	**1-2001**
5,674,787	**Zhao et al.**	**10-7997**

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 4, 18, 19, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin et al. (USPAT 5695810, Dubin) in view of Hong et al. (USPAT 6077774, Hong).

With regard to claims 1 and 3, Dubin discloses in figures 1 – 4 a method for forming conductors with high electromigration resistance. Dubin discloses in figures 1 – 4 forming a layer of dielectric (11) on a substrate. Dubin discloses in figures 1 – 4 forming at least one trench (8) in said layer of dielectric. Dubin discloses in figures 1 – 4 forming a metal liner (15) in said trench. Dubin discloses in figures 1 – 4 forming a conductor (16) on said metal liner filling said trench. Dubin discloses in figures 1 – 4 forming a planarized upper surface of said conductor planar with the upper surface of said layer of dielectric. Dubin discloses in figures 1 – 4 forming

a conductive film (17) over said upper surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Dubin does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 wherein a conductive film (34) has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Dubin in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claims 2 and 4, Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition whereby said upper surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

With regard to claims 18 and 20, Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 a method for forming conductors with high electromigration resistance. Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 forming a patterned conductor on a substrate. Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 forming a conductive film over said surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Dubin does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 forming a conductive film (34) over a surface of a conductor (30), the conductive film forming a metal to metal metallurgical bond and has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the

present invention to use the thickness of Hong for the conductive film of Dubin in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claims 19 and 21, Dubin discloses in figures 1 – 4 and column 7, lines 42 – 44 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition whereby said surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

Claims 1, 9, 10, 18, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maydan et al. (USPAT 6372633, Maydan) in view of Hong.

With regard to claim 1, Maydan discloses in figures 2, 3 and 6 – 7 a method for forming conductors with high electromigration resistance. Maydan discloses in figures 2, 3 and 6 – 7 forming a layer of dielectric (22) on a substrate. Maydan discloses in figures 2, 3 and 6 – 7 forming at least one trench (26) in said layer of dielectric. Maydan discloses in figures 2, 3 and 6 – 7 forming a metal liner (28) in said trench. Maydan discloses in figures 2, 3 and 6 – 7 forming a conductor (33) on said metal liner filling said trench. Maydan discloses in figures 2, 3 and 6 – 7 forming a planarized upper surface of said conductor planar with the upper surface of said layer of dielectric. Maydan discloses in figures 2, 3 and 6 – 7 forming a conductive film (34) over said upper surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Maydan does not disclose a thickness for the conductive film. Hong teaches in figure 1f,

column 1, lines 32 – 36 and column 5, lines 19 – 23 wherein a conductive film (34) has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Maydan in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 9, Maydan discloses in figures 2, 3 and 6 – 7, column 4, lines 62 – 67 and column 7, lines 9 – 12 wherein said conductive film is applied on the surface of said conductor by Chemical Vapor Deposition (CVD).

With regard to claim 10, Maydan discloses in figures 2, 3 and 6 – 7, column 4, lines 62 – 67 and column 7, lines 9 – 12 wherein said conductive film is W.

With regard to claim 18, Maydan discloses in figures 2, 3 and 6 – 7 a method for forming conductors with high electromigration resistance. Maydan discloses in figures 2, 3 and 6 – 7 forming a patterned conductor on a substrate. Maydan discloses in figures 2, 3 and 6 – 7 forming a conductive film over said surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Maydan does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 forming a conductive film (34) over a surface of a conductor (30), the conductive film forming a metal to metal metallurgical bond and has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Maydan in order to form a diffusion barrier with sufficiently low resistance

for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 26, Maydan discloses in figures 2, 3 and 6 – 7 wherein said conductive film is applied on the surface of said conductor by Chemical Vapor Deposition (CVD).

With regard 27, Maydan discloses in figures 2, 3 and 6 – 7 wherein said conductive film is W.

Claims 1, 2, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al. (USPAT 6180523, Lee) in view of Hong.

With regard to claim 1, Lee discloses in figures 1 – 8 a method for forming conductors with high electromigration resistance. Lee discloses in figures 1 – 8 forming a layer of dielectric (20) on a substrate. Lee discloses in figures 1 – 8 forming at least one trench (24) in said layer of dielectric. Lee discloses in figures 1 – 8 forming a metal liner (28) in said trench. Lee discloses in figures 1 – 8 forming a conductor (38) on said metal liner filling said trench. Lee discloses in figures 1 – 8 forming a planarized upper surface of said conductor planar with the upper surface of said layer of dielectric. Lee discloses in figures 1 – 8 forming a conductive film (46) over said upper surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Lee does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 wherein a conductive film (34) has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Lee in order

to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 2, Lee discloses in figures 1 – 8 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition whereby said upper surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

With regard to claim 18, Lee discloses in figures 1 – 8 a method for forming conductors with high electromigration resistance. Lee discloses in figures 1 – 8 forming a patterned conductor on a substrate. Lee discloses in figures 1 – 8 forming a conductive film over said surface of said conductor, said conductive film forming a metal to metal metallurgical bond. Lee does not disclose a thickness for the conductive film. Hong teaches in figure 1f, column 1, lines 32 – 36 and column 5, lines 19 – 23 forming a conductive film (34) over a surface of a conductor (30), the conductive film forming a metal to metal metallurgical bond and has a thickness of 9 nanometers. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of Hong for the conductive film of Lee in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip.

With regard to claim 19, Lee discloses in figures 1 – 8 wherein said step of forming a conductive film includes the step of forming said conductive film by electroless deposition

whereby said surface of said conductor is protected from oxidation and corrosion and provides high electromigration resistance and high resistance to thermal stress voiding.

Claims 5, 7, 22, 24, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dubin and Hong as applied to claims 1, 2, 18 and 19 above, and further in view of Zhao et al (USPAT 5674787, Zhao).

With regard to claims 5 and 22, Dubin discloses in figures 1 – 4 and column 6, lines 36 – 55 wherein said step of electroless deposition includes the steps of first immersing said substrate in a solution of metal ions whereby a layer of nanoparticles of metal are formed on said upper surface of said conductor. Dubin discloses in figures 1 – 4, column 6, lines 6 – 23 and column 7, lines 42 – 49 second immersing said substrate in an electroless complexed solution of metal ions and hypophosphite ions whereby the conductive film formed comprises a metal-phosphide conductive film on said upper surface of said conductor. Dubin teaches that the metal-phosphide conductive film is a barrier layer. It is not clear if Dubin and Hong teach annealing the metal-phosphide conductive film. Zhao teaches in figure 13; and column 8, lines 63 – 65 annealing a substrate in an inert atmosphere at a temperature of 200° C for 1 hour whereby excellent adhesion is obtained between a conductor (23) and a metal conductive film (24). It would have been obvious to one of ordinary skill in the art at the time of the present invention to anneal the metal-phosphide conductive layer of Dubin and Hong in order to improve the electrical properties of the plugs as stated by Zhao in column 3, lines 30 – 35. Dubin, Hong, and Zhao disclose the claimed invention except for the anneal at a temperature of at least 300° C and a time of at least 2 hours. It would have been obvious to one having ordinary skill in the art at the

time the invention was made to have the anneal at a temperature of at least 300° C and a time of at least 2 hours, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is further obvious in the method of Dubin, Hong, and Zhao that excellent adhesion is obtained between the conductor and the metal-phosphide conductive film during the anneal.

With regard to claims 7 and 24, Dubin teaches in column 7, lines 42 – 45 the conductive film is CoWP.

With regard to claims 37 and 38, Dubin discloses in figures 1 – 4, column 6, lines 6 – 23 and column 7, lines 42 – 49 wherein said electroless deposition comprises immersing said substrate in an electroless complexed solution of metal ions and hypophosphite ions whereby a metal-phosphide conductive film is formed on said upper surface of said conductor. It is not clear if Dubin and Hong teach annealing the metal-phosphide conductive film. Zhao teaches in figure 13; and column 8, lines 63 – 65 annealing a substrate in an inert atmosphere at a temperature of 200° C for 1 hour whereby excellent adhesion is obtained between a conductor (23) and a metal conductive film (24). It would have been obvious to one of ordinary skill in the art at the time of the present invention to anneal the metal-phosphide conductive layer of Dubin and Hong in order to improve the electrical properties of the plugs as stated by Zhao in column 3, lines 30 – 35. Dubin, Hong, and Zhao disclose the claimed invention except for the anneal at a temperature of at least 300° C and a time of at least 2 hours. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the anneal at a temperature of at least 300° C and a time of at least 2 hours, since it has been held that where the

general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is further obvious in the method of Dubin, Hong, and Zhao that excellent adhesion is obtained between the conductor and the metal-phosphide conductive film during the anneal.

Claims 8, 25, 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Hong as applied to claims 1, 2, 18 and 19 above, and further in view of Zhao.

With regard to claims 8 and 25, Lee discloses in figures 1 – 8 wherein said step of electroless deposition includes first immersing said substrate in a solution of metal ions whereby a layer of nanoparticles of metal are formed on the surface of said conductor. Lee discloses in figures 1 – 8 second immersing said substrate in an electroless complexed solution of metal ions and dimethylamino borane whereby the conductive film formed comprises a layer of metal-boron conductive film on said upper surface of said conductor. Lee teaches that the metal boron conductive film is a barrier layer. It is not clear if Lee and Hong teach annealing the metal boron conductive film. Zhao teaches in figure 13; column 3, lines 30 – 35; and column 8, lines 63 – 65 annealing a substrate in an inert atmosphere at a temperature of 200° C for 1 hour whereby excellent adhesion is obtained between a conductor (23) and a metal conductive film (24). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the annealing of Zhao in the method of Lee in order to improve the electrical properties of the plugs as stated by Zhao in column 3, lines 30 – 35. Lee, Hong, and Zhao discloses the claimed invention except for the anneal at a temperature of at least 300° C and a time of at least 2 hours. It would have been obvious to one having ordinary skill in the art at the time the

invention was made to have the anneal at a temperature of at least 300° C and a time of at least 2 hours, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233. It is further obvious in the method of Lee, Hong, and Zhao that excellent adhesion is obtained between the conductor and the metal-boron conductive film during the anneal.

With regard to claims 35 and 36, Lee teaches in column 7, line 59 wherein said conductive film is NiB.

(11) Response to Argument

A. Dubin and Hong Render Claims 1-4, 18, 19, 20 and 21 Obvious

With regard to appellant's argument that "Dubin seems to suggest a film of 150-200 nanometers thick (see column 6, lines 20 – 22)," it should be noted that the cited section of Dubin relates to a CoWP barrier layer 15. Dubin shows the deposition of this CoWP barrier layer 15 in figure 2. Element 15 of Dubin best corresponds to the claimed metal liner. The claimed thickness at issue is a thickness of a conductive film deposited over a planarized upper surface of a dielectric layer. As stated in the rejection, the conductive film (17) as shown in figure 5 of Dubin corresponds to the claimed conductive film. Dubin does not disclose a thickness for this conductive film 17. Therefore appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "Hong is not even properly combinable with Dubin since, among other things, Hong does not relate to CoWP films which are essential

according to Dubin," it should be noted that Hong is used to modify the conductive barrier layer of Dubin. It is not necessary for material of the conductive film 17 of Dubin and the conductive film 34 of Hong to be of the same material. Both of these films, in Dubin and Hong are used as a diffusion barrier over a planarized conductive line (16 in Dubin, and 30 in Hong). Hong is used to teach an appropriate thickness for the conductive film of Dubin. This is a proper combination for at least the reason that Dubin does not disclose a thickness for the conductive film. One of ordinary skill in the art would need to use a thickness of a conductive barrier film that is consistent with thicknesses of conductive barrier films that are known in the art. Hong teaches such a thickness of a barrier film. Dubin and Hong's use of different materials for their respective conductive films does not render the combination improper. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "Hong does not suggest employing electroless deposition for forming such a layer as required by Dubin," it should be noted that Hong is used to modify Dubin in as much as the thickness of the conductive layer. The combination does not require that Hong and Dubin use the same process to form the conductive layer. Hong is only relied on for teaching an appropriate thickness of the conductive film. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "there is no motivation listed in the prior art to combine Hong and Dubin," it should be noted that proper motivation is stated in the rejection as "in order to form a diffusion barrier with sufficiently low resistance for deep submicron copper interconnects as stated by Hong in column 1, lines 32 – 36. Deep submicron copper interconnects are desirable in order increase the speed of the chip." Appellant does not state any

reason why this motivation fails. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

B. Dubin in view of Hong and Zhao Render Claims 5, 7, 22, 24, 37, and 38 Obvious

With regard to appellant's argument that "Zhao is not even properly combinable with Dubin since, among other things, Zhao does not suggest CoWP film required by Dubin," it should be noted that the anneal of Zhao is used to improve the process of forming the metal-phosphide conductive barrier layer of Dubin and Hong. It is not necessary for material of the conductive film of Dubin and the conductive film 34 of Zhao to be of the same material. Both of these metal-phosphide films (17 in Dubin, and 24 in Zhao), are used as a diffusion barrier over a planarized conductive line (16, and 23 respectively). Zhao is used to suggest an improved way of forming the metal-phosphide conductive film of Dubin and Hong which includes an anneal. Appellant has not suggested any reason why using the anneal of Zhao in the method of Dubin in Hong would fail. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

C. Lee in view of Hong Render Claims 1, 2, 18 and 19 Obvious

With regard to appellant's argument that "Maydan does not relate to the problems addressed by the present invention and does not even remotely disclose the importance of the thickness of a metal barrier layer," it should be noted that U.S.C. section 103 does not require the prior art to address the same problems of the rejected claims. Further, the claims do not specify the importance of the thickness of a metal barrier layer. The originally filed specification also does not give reasons why the claimed range of 1 to 20 nanometers is critical. The burden is on the applicant to show the criticality of the claimed range. Hong shows that the claimed thickness

is readily attainable. Thus, the combination of Maydan and Hong is proper. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

D. Lee in view of Hong Render Claims 1, 2, 18, and 19 Obvious

With regard to appellant's argument that "Lee... fails to even remotely suggest the thickness of the conductive film as employed according to the present invention," it should be noted that Hong is again used for the thickness of the conductive film in the combination of Lee and Hong. Therefore, appellant's arguments are not persuasive and the rejection is proper.

With regard to appellant's argument that "Lee does not suggest forming a planarized upper surface of the conductor as recited in these claims," it should be noted that a quick review of figure 5 and column 9, lines 40 – column 10, lines 20 clearly shows that layers 20, 28, 34, and 38 define a planarized upper surface of the conductor (38) planar with the upper surface of the layer of dielectric (20). In this case the planarized upper surface of the conductor is formed during the deposition of the conductor. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "Hong does not suggest employing electroless deposition for forming the conductive layer as required by Lee," it should be noted that Hong is used to modify Lee in as much as the thickness of the conductive layer. The combination does not require that Hong and Lee use the same process to form the conductive layer. Hong is only relied on for teaching an appropriate thickness of the conductive film. Further with regard to appellant's argument that "Hong discusses problems of depositing their film, which are to be addressed by the particular techniques suggested therein," it should be noted that Hong mentions problems with chemical vapor deposition, sputtering, and evaporation techniques. Hong does

not suggest that any problems occur when using electroless deposition. Therefore, appellant's arguments are not persuasive and the rejection is proper.

E. Lee in view of Hong and Zhao Render Claims 8, 25, 35, and 36 Obvious

With regard to appellant's argument that "it seems logical that Lee would have discussed annealing if such were deemed appropriate for the process of Lee," it should be noted that the lack of discussion of annealing in Lee does not mean that Lee disregards annealing. Nowhere does Lee suggest that annealing would not be desirable. Therefore, even though Lee is aware of Zhao, there is nothing in Lee that teaches against the annealing of Zhao being a desirable process step. Appellant has not suggested any reason why the reasons for the combination fail. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "the thickness of Zhao leads "away from the thickness recited in the presented claims," it should be noted that the thickness of the layer in Zhao is not used in the present combination. Zhao is used to teach an annealing step that is beneficial to the process of Lee and Hong. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

With regard to appellant's argument that "Hong dies not suggest employing electroless deposition for forming such a layer as required by Dubin," it should be noted that Hong is used to modify Dubin in as much as the thickness of the conductive layer. The combination does not require that Hong and Dubin use the same process to form the conductive layer. Hong is only relied on for teaching an appropriate thickness of the conductive film. Therefore, appellant's arguments are not persuasive and the rejection is proper.

Relevant Case Law

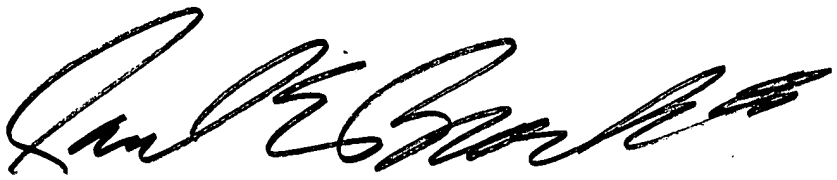
It is not clear how appellant's discussion of relevant case law directly relates to the issues at hand. Therefore, appellant's arguments are not persuasive, and the rejection is proper.

In conclusion, it should be noted that the originally filed disclosure, the claims, and all subsequent filings from the appellant fail to lay out reasons why the claimed thickness of 1 – 20 nanometers is a critical thickness. No evidence is given to show how a layer with a thickness outside of this range would fail to accomplish the stated benefits of the claimed conductive film. The burden to show criticality is the appellant's. Arguments are not evidence. Therefore, appellant's arguments are not persuasive, and the rejections are proper.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Paul E Brock II
November 17, 2004



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